Tutorial Xilinx ISE Download to NEXYS 2 Board <Release Version: 10.1>

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© Fall 2010 Baback Izadi Now that through simulation you have verified that your design is working, the next step is to download your design into the FPGA (Field Programmable Gate Array) of the NEXYS 2 Board. Save your schematic and return to the Project Navigator. Before proceeding, once again make sure that the FPGA device under sources is listed as XC3S50e-4fg320. If not double click on the device and make corrections as follows

Property Name	Value	
Product Category	All	~
Family	Spartan3E	~
Device	XC3S500E	~
Package	FG320	~
Speed	-4	*
Top-Level Source Type		~
Synthesis I ool	XST (VHUL/Verling)	×
Simulator	ISE Simulator (VHDL/Verilog)	-
Preferred Language	VHDL	~
Enable Enhanced Design Summa	ary 🔽	
Enable Message Filtering		

Now under Sources window, use the drop box to select Synthesis/Implementation. Then, select the schematic to be downloaded and double click on Create New Source under Processes. This will open a dialog box. Select Implementation Constraints File, enter a file name and click Next.



This opens up the fo	ollowing dialog box		
🚾 Xilinx - ISE - C:\Documents and S	ettings\n01914860\Desktop\MyALU\My	yALU.ise - [Design Summary]	
🔉 File Edit View Project Source Proces	s Window Help		
1 🗅 🖻 🖥 🕼 😓 11 X 🖻 🗎 🗙	12 @ 🗹 🗄 🗭 🖉 🗶 🗶 🖉	🔊 i 🔁 🖻 💷 🗖 i 🌽 😽 i i	M 🕷 💽 🖌
Sources >	FPGA Design Summary		MyALU Pro
Sources for: Implementation	Design Overview	Project File:	MyALU.ise
────────────────────────────────────	Summary	Module Name:	MyFullAdder
Acussulation and a second	Module Level Utilization	Target Device:	xc3s500e-4fg320
E CONTRACTOR OF CONTRACTOR	Timing Constraints	Product Version:	ISE 10.1.03 - Foundation Simulator
	Pinout Report	Design Goal:	Balanced
🕫 Source 👔 Files 👩 Snapshi 👔 Librar	ie 📄 Clock Report	Design Strategy:	Xilinx Default (unlocked)
Processes	Crois and warnings Synthesis Messages		
Processes for: MyFullAdder Add Existing Source Create New Source View Design Summary Design Utilities User Constraints Osynthesize - XST Oglinplement Design Oglinplement Design Configure Target Device	New Source Wizard - Summary Project Navigator will create a new skeleton so Add to Project: Yes Source Directory: C:Nocuments and Settings' Source Type: Implementation Constraints File Source Name: constraints.ucf Association: MyFullAdder Show Errors	urce with the following specifications: n01914860\Desktop\MyALU <back< td=""><td>Finish Cancel</td></back<>	Finish Cancel
	Show Warnings	Depart Name Claim	Detailed Repor
	Show Failing Constraints	Report Name Status	Lienerated

Click Finish!

The constraints file, constraints.ucf has been created. Select constraints.ucf in the source window and then go to Edit Constraints in the process window.



This opens a window to edit constraints, where you can assign inputs and outputs to appropriate switches and LEDs in the FPGA chip.



After writing the constraints save it.

Next, select MyFullAdder.sch in the source window and then right click on Generate Programming File and click on Properties



Go to Startup options in the properties and select JTAG clock and click ok.



Double click on Generate Programming File. Check the transcript window. If it shows

Process "Generate Programming File" completed successfully, it means bit file is created. If there are errors, correct them and repeat the process.



Now, your BIT file is ready to be downloaded to the Digilent NEXYS 2 board.

In Desktop, under Programs, go to Engineering Software \rightarrow Digilent \rightarrow Adept \rightarrow Adept and click on it



The following window should open.

🛕 Digilent Adept		
NEXYS 2	Connect: Nexys2	~
	Product: Nexys2 - 500	
Config Test Register I/O File I/O	I/O Ex Settings	
FPGA ×C3S500E	Browse Program	m
PROM XCF04S	Browse Program	m
Initiali	ze Chain	
Board information loaded.		^
Found device ID: 41c22093 Initialization Complete.		
Device 1: XC35500E Device 2: XCF045		
		~

Click on Initialize Chain, which loads the board's information. Open your bit file using FPGA (XC3S500E) and click on Program.

🛆 Digilent Adept	
NEXYS 2	Connect: Nexys2 Product: Nexys2 - 500
Config Test Register I/O File I/O	I/O Ex Settings
FPGA XC3S500E myfulladder.bit	Browse Program
PROM XCF04S	Browse Program
Initializ	ze Chain
Initializing Scan Chain Found device ID: f5046093 Found device ID: 41c22093 Initialization Complete. Device I XC35500F	×
Device 2: XCF045	 ⊻

This downloads your bit file into the NEXYS 2's FPGA chip.

If everything is successful, you will get the following message "programming successful".

nfig Tes	t Register I/	O File I/O	I/O Ex Se	ttings	
FPGA XC3S500E	myfulladder.bit		*	Browse	Program
PROM XCF04S			*	Browse	Program
		Initialize (Chain		

Now flip the switches on the board and see your design come to life!

Additional Information of NEXYS 2 board

The Nexys2 board includes several input devices, output devices, and data ports, allowing many designs to be implemented without the need for any other components.



Four pushbuttons and eight slide switches are provided for circuit inputs. Pushbutton inputs are normally low, and they are driven high only when the pushbutton is pressed. Slide switches generate constant high or low inputs depending on their position. Pushbutton and slide switch inputs use a series resistor for protection against short circuits (a short circuit would occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The Nexys2 board contains a four digit common anode seven segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment.

